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TSMC-00-084

April 3, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/082,021 02/21/02

Kuei-Ying Lee et al.

NOVEL PRODUCTS DERIVED FROM EMBEDDED FLASH/EEPROM PRODUCTS

Grp. Art Unit: 2811

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on April 10, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 4/10/02

U.S. Patent 6,021,079 to Worley, "Fast, Low cost Method of Developing Code for Contact Programmable ROMs," discloses an antifuse PROM which is embedded into a conventional CMOS process with some additional process steps and additional area for the wire circuitry.

U.S. Patent 6,037,222 to Huang et al., "Method for Fabricating a Dual-Gate Dielectric Module for Memory Embedded Logic Using Salicide Technology and Polycide Technology," discloses a method for fabricating a dual-gate dielectric module for memory embedded logic using salicide technology and polycide technology.

U.S. Patent 6,020,241 to You et al., "Post Metal Code Engineering for a ROM," teaches a threshold voltage implant method of manufacturing a ROM that is code implanted late in the process after the first level metal, thus reducing the TAT to ship a customer order.

U.S. Patent 6,041,008 to Marr, "Method and Apparatus for Embedded Read Only Memory in Static Random Access Memory," discloses a ROM embedded SRAM utilizing an existing support circuitry of the SRAM array.

U.S. Patent 5,751,040 to Chen et al., "Self-Aligned Source/Drain Mask ROM Memory Cell Using Trench Etched Channel," discloses a self-aligned source/drain mask ROM memory cell using trench etched channel.

U.S. Patent 5,938,774 to Hsu, "Apparatus for Repairing Faulty Program Segments in Embedded Microprocessor Systems," discloses an apparatus for repairing faulty program segments in embedded microprocessor systems.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-00-084	10/082,021
Applicant: Kuei-Ying Lee et al.	
Filing Date: 02/21/02	Group Art Unit: 2811

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6021079	2/1/00	Worley	365	225.7	5/13/98
	6037222	3/14/00	Huang et al.	438	257	5/22/98
	6020241	2/1/00	You et al.	438	278	12/22/97
	6041008	3/21/00	Marr	365	225.7	5/13/98
	5751040	5/12/98	Chen et al.	257	332	9/16/96
	5938774	8/17/99	Hsu	714	6	9/30/97

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.